REMARKS

Claims 1-8, 11 and 12 are pending in this application. By this Preliminary Amendment, claims 1-8 and 11 are amended and claims 9, 10 and 13-16 have been cancelled. Attached hereto is a marked-up version of the changes made to the claims by this Preliminary Amendment. The attached page is captioned **"Version with markings to show changes made to the specification and claims"**.

This application claims priority under 35 USC §120 from Application No. 09/181,676, filed October 29, 1998, which in turn claims priority from Japanese Patent Application No. 09/296,653, filed October 29, 1997.

A prompt examination of the merits is earnestly solicited.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.36683VX1).

Respectfully submitted,

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<u>**VERSION WITH MARKINGS TO SHOW CHANGES MADE IN THE**</u>

<u>**SPECIFICATION AND CLAIMS**</u>

<u>**IN THE SPECIFICATION:**</u>

The following new paragraph has been added on page 1, before line 1.

--This application is a Rule 53(b) continuation of U.S. Patent Serial Number 09/181,676, filed October 29, 1998, the subject matter of which is incorporated herein by reference. --

<u>**IN THE CLAIMS:**</u>

Claims 9-10 and 13-16 have been cancelled.

Claims 1-8 and 11 have been amended as follows:

1. (Amended) An information processing system comprising:

a processor;

a memory; and

a memory controller connected with said processor via a first bus and

connected with said memory via a second bus for controlling said memory,

[wherein] said memory controller [comprises] <u>further comprising:</u> a buffer [memory

and]<u>,</u>

a control circuit, and

[said control circuit is controlled, before a memory access is carried out from said

processor, to estimate an address to be possibly next accessed on the basis of addresses

accessed in the past and to prefetch data stored in said memory into said buffer memory, in

accordance with said estimated address wherein said data has a data size of twice or more an

access unit of said processor]

6

an access judging circuit, wherein;

said control circuit estimates a most probable address to be accessed next in said memory,

said access judgement circuit prefetches a data stored in said most probable address of the memory into the buffer memory, before a memory access is carried out from said processor.

2. (Amended) An information processing system according to claim 1, wherein said memory controller comprises a direct path for transmitting data directly to said processor from said memory therethrough; said control circuit, when the access from said processor hits data within said buffer [memory], is controlled to transfer the data to said processor, whereas, said control circuit, when the access from said processor fails to hit data within said buffer [memory], is controlled to transfer data within said memory to said processor via said direct path.

3. (Amended) An information processing system according to claim 1, wherein said memory stores an instruction code to be executed on said processor therein, and said control circuit prefetches the instruction code into said buffer [memory].

4. (Amended) An information processing system according to claim 1, wherein said memory stores therein an instruction code to be executed on said processor and operand data, and said control circuit prefetches the instruction code and operand data into said buffer [memory].

5.   (Amended)   An information processing system according to claim 1,
comprising a plurality of [buffer memories] <u>buffers</u> into which data of said access unit is
prefetched, and wherein said control circuit controls to transfer data already stored in said
plurality of [buffer memories] <u>buffers</u> to said processor in an order different from an address
order.

6.   (Amended)   An information processing system according to claim 1,
wherein said memory controller has an instruction decoder and a branching buffer [memory],
and said control circuit, when said instruction decoder detects a branch instruction, prefetches
an instruction code as a branch destination into said branching buffer [memory] and, when an
access is made from said processor to the instruction code, judges whether or not the
instruction code hits data within said buffer [memory] and said branching buffer [memory].

7.   (Amended)   An information processing system according to claim 1,
wherein said memory controller has a register for instructing start or stop of the prefetch to
said buffer [memory].

8.   (Amended)   An information processing system according to claim 1,
wherein said control circuit is controlled in its initial state to prefetch data already stored at a
pre-specified address into said buffer [memory].

11.   (Amended)   An information processing system according to claim 1, wherein said processor has an internal cache, and said control circuit is controlled to prefetch data having a data size of twice or more a line size of said internal cache into said buffer [memory].